## 26.10 A 1.2V Dual-Mode GSM/WCDMA ΔΣ Modulator in 65nm CMOS

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Multi-band ADCs have gained a lot of interest in the recent years, since they enable a flexible way of realizing multimode receivers. For multimode ADC applications, ΔΣ modulators implemented in deep sub-micron technology are preferred, since they enable robust and cost-effective designs with performance trade-offs in terms of OSR and power consumption [1, 2, 3]. In this paper, a dual-mode ΔΣ modulator designed for a GSM/WCDMA direct-conversion receiver is described. The DR targets for this direct-conversion receiver are 84dB over 100kHz GSM band and 50dB over 1.92MHz WCDMA band with analog filtering.

In deep sub-micron technologies it is advantageous to use second-order loops, if low power consumption is targeted [1, 2, 3]. For wideband operation, multi-bit quantization or MASH structures are preferred [1, 2, 3]. However, with multi-bit modulators, the internal DAC is not inherently linear. Furthermore, MASH structures are sensitive to circuit non-idealities and require amplifiers with high DC gain [1]. Nevertheless, both methods increase the circuit complexity and power consumption.

To achieve low power consumption and good stability, a classical second-order single-bit ΔΣ modulator is chosen. To meet the DR requirements without multi-bit quantization in both the GSM and WCDMA bands, the sampling clock frequencies are chosen based on WCDMA requirements to be 48MHz and 96MHz resulting in OSRs of 240 and 25, respectively. This choice enables the shift from WCDMA to GSM mode by merely dividing the sampling clock by two. In addition, with integer OSRs, the implementation of the following digital circuitry is simple and power efficient.

The schematic of the implemented SC ΔΣ modulator is shown in Fig. 26.10.1. The input sampling capacitor is shared with the feedback DAC to reduce kT/C noise. To achieve a 14b dynamic range, the input sampling capacitor is sized with some margin to be 500fF. At the input of the second integrator a separate feedback DAC capacitor is used to implement the required scaling factors at the modulator feedback loop. However, the increase in input-referred noise is small, since the noise of the second feedback DAC capacitor is divided with the gain of the first integrator. To reduce the signal-dependent charge injection of the switches, bottom plate sampling is utilized. The non-overlapping clock signals are generated using a simple circuit constructed of logic gates.

The switches are implemented using core transistors without clock boosting. However, to reduce the nonlinear distortion of the critical switches, the input sampling switches of both integrators are implemented as bootstrapped switches [4], as shown in Figs. 26.10.1 and 26.10.2. This structure enables a rail-to-rail operation of the input switch with a long-time reliability. To save silicon area, the pre-charge capacitor is implemented with a PMOS-transistor.

The reference voltages are chosen to be 0V and 800mV for two reasons. First, with a low supply voltage, the operation of the critical input signal sampling switches improves when the input common mode (CM) level (IAGND in Fig. 26.10.1) is lower than a middle of the supply voltage. Secondly, to reduce the amplifier flicker noise, PMOS input transistors are used, resulting in the optimum input CM level of around 400mV. It should be noted that only one reference voltage (800mV) is required in addition to ground.

With a low supply voltage, the amplifier output swing should be maximized to minimize noise. Furthermore, due to the small output resistance of deep sub-micron transistors, the achievable gain from a single transistor is moderate. Thus, a two-stage amplifier with a common-source output stage is preferred. Hence, a two-stage Miller-compensated operational amplifier shown in Fig. 26.10.3 is utilized. The Miller compensation is implemented with a pole splitting capacitor $C_C$ and compensation NMOS resistor $M_{11}$. PMOS input transistors are chosen to reduce the flicker noise and to operate well with a low input CM level. The output CM level is chosen in the middle of the supply voltages to maximize the output swing. The designed differential output swing is $1600mV_{pp}$.

The amplifier utilizes two CM feedbacks (CMFBs) for fast operation, one for each stage. The input stage has a continuous-time CMFB. It is implemented using NMOS-transistors ($M_4$, $M_5$) as resistors to detect the CM levels at the output of the input stage. In addition, there are constant-biased NMOS load transistors to attenuate the current through CMFB to one fifth of the input transistors bias current. This increases the gain of the input stage and the operation is more stable. The output stage utilizes a SC CMFB. The designed amplifier has a 57dB DC gain and a 45° phase margin. The GBW of the first and second integrator are 750MHz and 400MHz, while drawing a current of about 1.3mA and 0.6mA, respectively.

The quantizer is implemented as a regenerative type comparator followed by an RS flip-flop. The quantizer output is buffered with cross-coupled NAND-gates to keep the logic value unchanged during the sampling phase.

The measured spectrum of the modulator clocked at 48MHz in GSM mode is shown in Fig. 26.10.4. The spectrum is calculated from 262144-point FFT plot of the output data using Kaiser window (β=13). The input sine wave is -3dBFS at 19.037kHz frequency. When clocked at 48MHz, the measured peak SNDR is 84dB for GSM mode, while consuming 3.3mW. Sampling at 96MHz doubles the OSR in the WCDMA mode, and improves the peak SNDR for WCDMA to 49dB and increases power dissipation to 3.6mW. The measured SNDR versus input amplitude is shown in Fig. 26.10.5.

The prototype is fabricated in a 65nm CMOS technology, using only metal-to-metal capacitors. The chips are directly bonded on a PCB. The total core area of the modulator is $0.1mm^2$ (Fig. 26.10.7), and it draws 2.75mA and 3.0mA from a 1.2V supply in GSM and WCDMA modes, respectively. The overall performance is summarized in Fig. 26.10.6.

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*References:*
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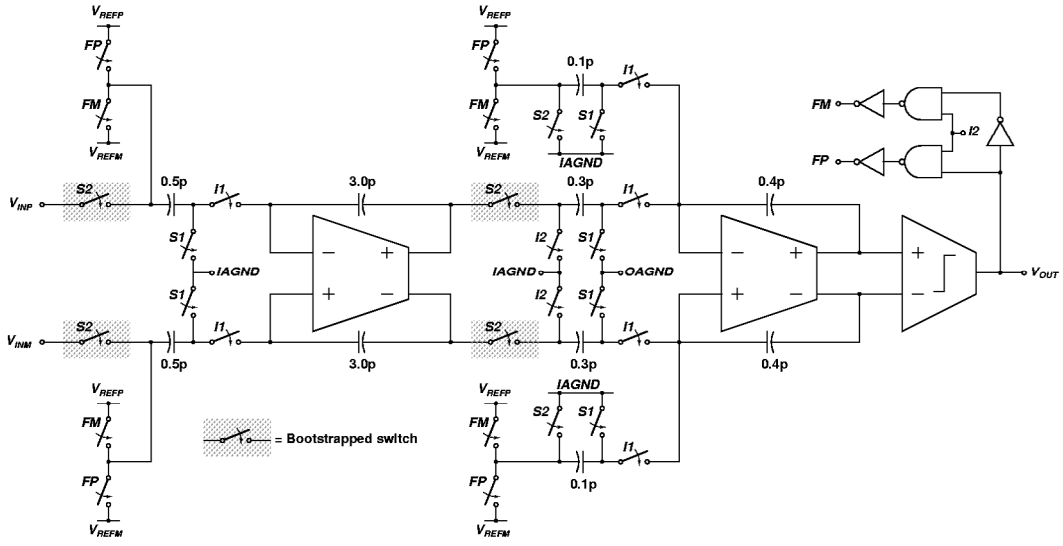


Figure 26.10.1: Second order ΔΣ modulator schematic.

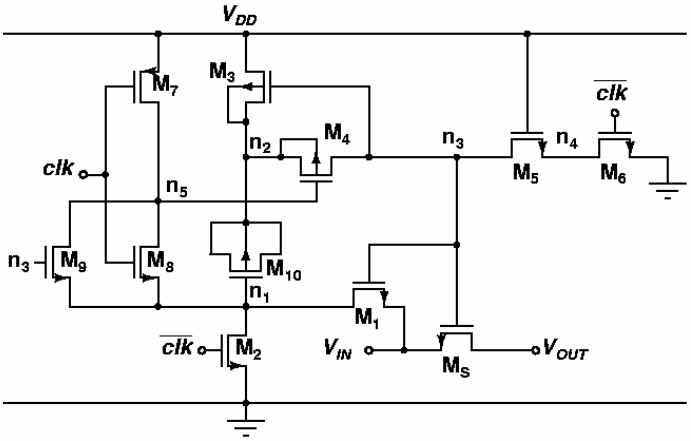


Figure 26.10.2: Bootstrapped switch schematic [4].

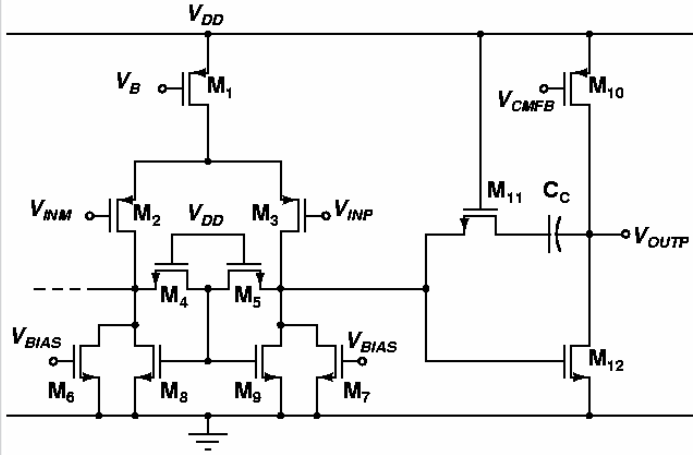


Figure 26.10.3: Operational amplifier schematic (one side).

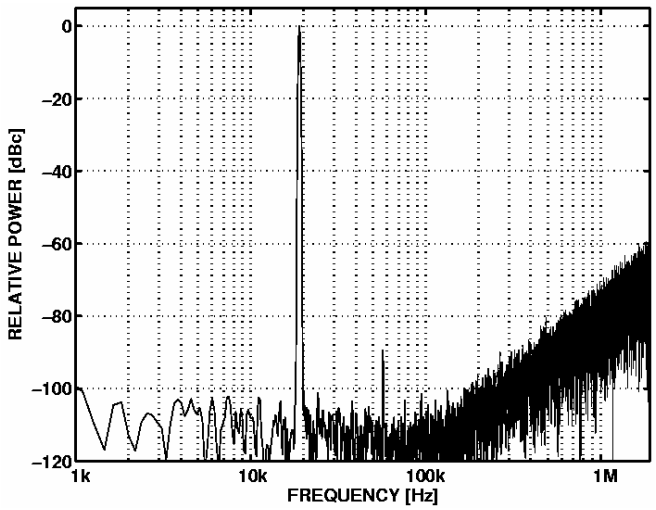


Figure 26.10.4: Measured output spectrum in GSM mode ($f_S$=48MHz).

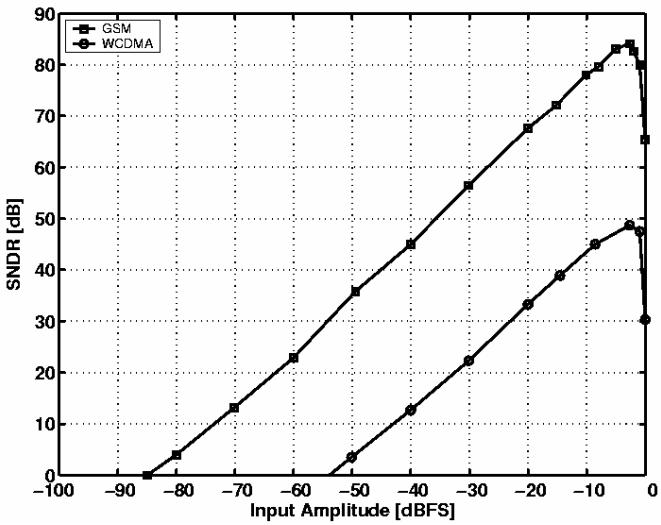


Figure 26.10.5: Measured SNDR versus input amplitude.

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| | GSM | WCDMA |
|---|---|---|
| Technology | 65nm Digital CMOS | |
| Core area | 0.1 $mm^2$ | |
| Differential Input Range | 1600 $mV_{PP}$ | |
| Supply Voltage | 1.2 V | |
| Power Consumption | 3.3 mW | 3.6 mW |
| Signal Bandwidth | 100 kHz | 1.92 MHz |
| Sampling Frequency | 48 MHz | 96 MHz |
| Peak SNDR | 84 dB | 49 dB |
| Dynamic Range | 85 dB | 54 dB |

**Figure 26.10.6: Performance summary.**

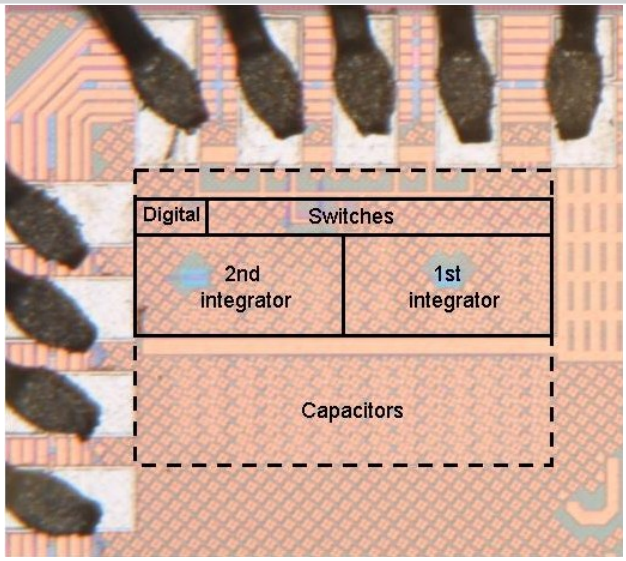


**Figure 26.10.7: Chip micrograph.**

 